We claim:

1. In a data transmission system with at least two subscribers, a memory device to be connected, for serial data transfer of binary data objects of a predetermined data width, between the at least two subscribers, comprising:

a multiplicity of memory objects each being identifiable by a respective address;

each said memory object having a data width being at least as large as a predetermined data width of a data object intended for data transfer;

at least one FIFO structure containing a plurality of said memory objects and transmitting data in a data-controlled data transfer controlled by the data objects being transmitted.

2. The memory device according to claim 1, wherein said memory objects are equal in size.

3. The memory device according to claim 1, wherein the subscribers in the data transmission system are operated at mutually different data transmission rates.

4. The memory device according to claim 1, wherein each of the subscribers is adapted to be a data transmitter and a data receiver.

5. The memory device according to claim 1, wherein each of said memory objects comprises:

an identification region containing the respective address of said memory object;

a data region storing the data objects; and

a control region containing monitoring and control functions for the data transfer.

6. The memory device according to claim 1, wherein each of said FIFO structures has a data-controlled FIFO fill-level register indicating how many of said memory objects in said FIFO structure have already been written to and/or which are empty.

7. The memory device according to claim 1, wherein each said memory object includes a node selection register indicating a subscriber to which the respective said memory object is assigned.

8. The memory device according to claim 7, wherein a content of said node selection register is configurable via at least one of the subscribers and a central processing unit.

9. The memory device according to claim 1, wherein each said memory object includes a gateway control register defining an operating mode of the respective said memory object.

10. The memory device according to claim 9, wherein a content of said gateway control register is configurable via at least one of the subscribers and a central processing unit.

11. The memory device according to claim 1, wherein each said memory object includes a node selection register indicating a subscriber to which the respective said memory object is assigned, and a gateway control register defining an operating mode of the respective said memory object, and wherein a content of said gateway control register and a content of said node selection register are configurable via at least one of the subscribers and a central processing unit.

12. A method of operating the memory device according to claim 1, which comprises:

defining a first operating mode wherein the following method steps are performed:

(a) providing a FIFO structure;

(b) defining the first subscriber as a data transmitter and successively writing, with the data transmitter, a plurality of data objects to successively arranged memory objects in the FIFO structure;

(c) repeating the writing step until all the memory objects in the FIFO structure have been written to or all the data

objects intended for data transfer have been stored in respective memory objects in the FIFO structure;

(d) releasing the FIFO structure for a read operation; and

(e) defining the second subscriber as a data receiver reading, with the data receiver, the data objects that have just been written to the respective memory objects in the FIFO structure, in a same sequence as they were written in the writing step.

13. The method according to claim 12, which comprises:

defining a second operating mode wherein the following method steps are performed:

(a) providing a memory object pair with two memory objects;

(b) writing, with the data transmitter, a data object intended for data transfer to a first memory object in the memory object pair;

(c) copying the data object from the first memory object to a second memory object in the memory object pair;

(d) reading, with the data receiver, the data object from the second memory object.

14. The method according to claim 13, which further comprises: defining a third operating mode, wherein a first FIFO structure and a second FIFO structure or an individual memory object are provided, wherein the first FIFO structure is operated in the first operating mode for data buffering of the data objects to be read in or read out, and wherein the second FIFO structure or the individual memory object is operated in the second operating mode for reading out or reading in the corresponding data objects.

15. The method according to claim 12, which further comprises defining a fourth operating mode wherein the following method steps are performed:

(a) providing a memory object;

(b) writing, with the data transmitter, a data object intended for data transfer to the memory object;

(c) releasing the memory object for reading; and

(d) reading, with the data receiver, the data object from the memory object.

16. The method according to claim 14, which comprises selectively operating the memory cells in the FIFO structure under data control both in the first operating mode, in the second operating mode, and, selectively, in the third operating mode.

17. The method according to claim 15, which comprises selectively operating the memory objects under data control in any of the first operating mode, the second operating mode, the third operating mode, and the fourth operating mode.

18. The method according to claim 13, which comprises assigning addresses to the respective first memory objects of the FIFO structure that is being operated in the first memory mode with even numbers, and assigning addresses of the respective first memory objects of a memory object pair being operated in the second operating mode with odd numbers.

19. The method according to claim 12, which comprises holding off with reading the memory objects that have been written to until after a request signal from a central processing unit or from the data receiver.

20. The combination according to claim 1, wherein the memory device is integrated in a bridge module, the at least two subscribers are bus systems, and the bridge module is connected between the subscribers.

21. The combination according to claim 1, wherein the first subscriber is a central processing unit, and the second subscriber is coupled to a data bus of a bus system.

22. A ~~CAN~~ bus system, comprising: at least one memory device according to claim 1.